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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,735	05/11/2001	Mototsugu Okushima	NE212-US	4991

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/852,735	OKUSHIMA, MOTOTSUGU
	Examiner	Art Unit
	ori nadav	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *72-85* is/are pending in the application.

4a) Of the above claim(s) *80-85* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *72-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of the embodiment of figure 25 (claims 73-79) in the reply filed on 01/21/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because figure 25 does not include the following reference sign 21 mentioned in the description (reference sign 11 of trigger element 310 should be 21). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 74-75 are objected to because of the following informalities: In claim 74, line 3, the term "transistors" should read "transistor".

Claim 74 recites the limitation "said plural bipolar transistors" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 73-79 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed,

had possession of the claimed invention. There is no support in the specification, as filed, for a vertical bipolar transistor being formed on a semiconductor substrate for discharging accumulated electric charge from a surface layer of said semiconductor substrate towards depth direction of said semiconductor substrate, as recited in claim 73.

Claims 73-79 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of vertical bipolar transistor leads out collector electrodes through a collector-connection well, as recited in claim 73, are unclear as to how a vertical bipolar transistor can lead out collector electrodes, which are located above the substrate through a collector-connection well which is located in the substrate.

The claimed limitations of collector layers of said plural bipolar transistors are formed as a common layer, as recited in claim 75, are unclear as to whether said plural bipolar transistors are the vertical bipolar transistors recited in claim 74, and how said plural bipolar transistors are formed as a common layer since each bipolar transistor comprises a separate collector layer 17 and all the collector layers are connected by well 14.

The claimed limitations of said semiconductor substrate of a first conductive type and said anode are insulated in said second conductive region, as recited in claim 77, are unclear as to how the semiconductor substrate and the anode can be insulated in a

second conductive region since the anode and the second conductive region are formed in the semiconductor substrate.

The claimed limitations of said semiconductor substrate of a first conductive type and said anode are insulated in said second conductive region simultaneously formed with said collector of said transistor, as recited in claim 77, are unclear as to which elements are simultaneously formed with said collector of said transistor.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 73-79, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwai et al. (5,648,676) in view of Li et al. (5,623,387).

Iwai et al. teach in figure 2a and related text an ESD protection device for protecting a transistor from an overvoltage, said ESD protection element comprising:

a vertical bipolar transistor 14 being formed on a semiconductor substrate 19 for discharging accumulated electric charge from a surface layer of said semiconductor substrate towards depth direction of said semiconductor substrate, wherein

said vertical bipolar transistor leads out collector electrodes through a collector-connection region 20a and

said vertical bipolar transistor has a collector 20a and a base 29a formed in a same region.

Iwai et al. do not teach an ESD protection device connected between a CMOS transistor and a pad for protecting said CMOS transistor from an overvoltage applied to said pad, and a collector-connection region being a well.

Li et al. teach in figure 4a an ESD protection device connected between a CMOS transistor T3, T4 and a pad 101 for protecting said CMOS transistor from an overvoltage applied to said pad.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Iwai et al.'s ESD protection device to protect a CMOS transistor from an overvoltage applied to a pad, and to form the collector-connection region as a well, in order to use the ESD device in an application which requires protection to a CMOS transistor from an over-voltage applied to a pad, and in order to improve the electrical isolation of the device by forming the collector-connection region in a conventional method (as a well), respectively.

Regarding the process limitations recited in claims 73 and 76 ("forming the collector and the base by using the same mask", and "a first conductive region formed simultaneously with said base of said vertical bipolar transistor on a surface of a semiconductor substrate and a second conductive region simultaneously formed with an emitter on a

surface of said first conductive region"), these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claim 74, Li et al. teach an ESD protection device comprising plural of bipolar transistors adjacent to each other. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use plural of vertical bipolar transistors adjacent to each other in Iwai et al.'s ESD protection device in order to provide better protection to the internal circuit.

Regarding claim 75, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form collector layers of said plural bipolar transistors

as a common layer in Iwai et al.'s ESD protection device in order to simplify the processing steps of making the device.

Regarding claims 76 and 77, Li et al. teach a trigger device for switching said bipolar transistor of said ESD protection device using an application of an over-voltage as a trigger, wherein said trigger device comprises:

a diode 124 having, in a joined state, a first conductive region formed simultaneously with said base of said vertical bipolar transistor on a surface of a semiconductor substrate and a second conductive region simultaneously formed with an emitter on a surface of said first conductive region, wherein:

in the diode of said trigger device; said first conductive region forms an anode and said second conductive region forms cathode; and said semiconductor substrate of a first conductive type and said anode are insulated in said second conductive region simultaneously formed with said collector of said transistor.

Regarding claims 78 and 79, in the trigger device of prior art's device, the anode is connected with said base of said vertical bipolar transistor and said cathode is connected with said collector said vertical bipolar transistor since all the circuit elements are electrically connected to each other, wherein Iwai et al. teach in figure 5a the base 10a of the vertical bipolar transistor is connected with a ground terminal through a resistor 61.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956.**

O.N.
3/28/05

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800